Oregon Institute of Technology
Computer Systems Engineering Technology Department

Embedded Systems Engineering Technology Program Assessment

2008-09

I. Introduction

The Embedded Systems Engineering Technology (ESET) program was proposed to OUS in spring of 2006 and approved in August, 2006. The curriculum for the ESET program is common with the hardware and software programs for the freshman year. The sophomore year of the ESET program has been constructed to mirror the track through both the Computer Engineering Technology (CET) and Software Engineering Technology (CET) programs, called the Dual Degree program. The ESET program junior year is when ESET students get instruction specific to topics of embedded systems engineering. These courses were taught for the first time in fall, 2008.

II. Mission, Objectives and Program Student Learning Outcomes

The mission of the Embedded Systems Engineering Technology (ESET) Degree program within the Computer Systems Engineering Technology (CSET) Department at Oregon Institute of Technology is to prepare our students for productive careers in industry and government by providing an excellent education incorporating industry-relevant, applied laboratory based instruction in both the theory and application of embedded systems engineering. Our focus is educating students to meet the growing workforce demand in Oregon and elsewhere for graduates prepared in both hardware and software aspects of embedded systems. Major components of the ESET program's mission in the CSET Department are:

I. To educate a new generation of Embedded Systems Engineering Technology students to meet current and future industrial challenges and emerging embedded systems engineering trends.

II. To promote a sense of scholarship, leadership, and professional service among our graduates.

III. To enable our students to create, develop, apply, and disseminate knowledge within the embedded systems development environment.

IV. To expose our students to cross-disciplinary educational programs.

V. To provide government and high tech industry employers with graduates in embedded systems engineering and related professions.

Program Educational Objectives

The Program Educational Objectives reflect those attributes a student of the ESET program will practice in professional endeavors.

A. Graduates of the embedded program are expected to understand societal impact of embedded systems and technological solutions.

B. Graduates of embedded degree program are expected to do hardware/software co-design for embedded systems. Graduates will continue to develop skills in analysis, approach, optimization, and implementation of embedded systems.

C. Graduates of the embedded program are expected to obtain the knowledge, skills and capabilities necessary for immediate employment in embedded systems. Embedded Systems is a profession increasingly driven by advances in technology, therefore graduates are expected to obtain the necessary life-long learning skills to enable them to be able to adapt to a changing environment.

D. Graduates of the embedded program are expected to develop a broad base of skills. These skills will prepare them for professional practice: 1) as embedded engineers, 2) participants in embedded development teams, and 3) effective communicators within a multidisciplinary team.

E. Graduates of the embedded program are expected to acquire knowledge of management and marketing of embedded projects and products and to prepare for series production.

Program Student Learning Outcomes

Embedded Systems Engineering Technology baccalaureate graduates will be engaged in:

1. Application of mathematics including differential and integral calculus, probability, and discrete mathematics to hardware and software problems (Objectives C, D, E).

2. Application of project management techniques to embedded systems projects (Objectives C and D).

3. Application of knowledge of embedded systems engineering technology, along with some specialization in at least one area of computer systems engineering technology. (Objective D)

4. A broad education and knowledge of contemporary issues necessary to reason about the impact of embedded system based solutions to situations arising in society. (Objective A)

5. Identification and synthesis of solutions for embedded systems problems. (Objective B, C)

6. Design, execution and evaluation of experiments on embedded platforms. (Objective C, D)

7. Analysis, design and testing of systems that include both hardware and software. (Objective B, D)

8. Documenting the experimental processes and to writing of satisfactory technical reports/papers. (Objective D, E)

9. Delivery of technical oral presentations and interacting with a presentation audience. (Objective D, E)

10. Recognition for and the motivation to further develop their knowledge and skills as embedded engineering advances occur in industry. (Objective C)

11. Working effectively, independently, and in multi-person teams. (Objective D)

12. Professional and ethical execution of responsibilities. (Objective A, D)

III. Three-Year Cycle for Assessment of Student Learning Outcomes

Assessment activities for the ESET program will begin Fall, 2008. Table 1 presents planned learning outcome assessment on a three year cycle. The number in the cells of the table corresponds to the ISLO defined for the OIT assessment cycle.

Table 1: Baccalaureate Outcome Assessment Timeline

#	**Learning Outcomes**	**08-09**	**09-10**	**10-11**	**11-12**	**12-13**	**13-14**
1	The ability to apply mathematics including differential and integral calculus, probability, and discrete mathematics to hardware and software problems.	**6**			**6**		
2	An ability to apply project management techniques to embedded systems projects.		**2, 3**			**2, 3**	
3	Knowledge of embedded systems engineering technology, along with some specialization in at least one			**5**			**5**

	area of computer systems engineering technology.						
4	A broad education and knowledge of contemporary issues necessary to reason about the impact of embedded system based solutions to situations arising in society.		**3, 8**			**3, 8**	
5	The ability to identify and synthesize solutions for embedded system problems.			**4**			**4**
6	The ability to design, conduct and evaluate the results of experiments on embedded platforms.	**7**			**7**		
7	The ability to analyze, design and test systems that include both hardware and software.	**7**			**7**		
8	The ability to document experimental processes and to write satisfactory technical reports/papers.			**1**			**1**
9	The ability to make technical oral presentations and interact with an audience.			**1**			**1**
10	The recognition for and the motivation to further develop their knowledge and skills as embedded engineering advances occur in industry.			**5**			**5**
11	The ability to work effectively independently and in multi-person teams.		**2**			**2**	
12	An understanding of professional and ethical responsibility.		**3, 8**			**3, 8**	

To summarize, Table 2 shows the outcomes (identified by number only) that will be assessed for each of the next three years.

Table 2: Summary of Assessment Timeline

Academic Year	Outcomes
2008-09	1, 6, 7
2009-10	2, 4, 11, 12
2010-11	3, 5, 8, 9, 10

Target courses where the assessment tools were to be applied for the 2008-09 academic year are summarized in Table 3.

Table 3: 2008 – 2009 Summary Courses of Assessment Application

Outcome	Courses	Term
1	CST 162	Fall
	CST 466	Spring
	CST 418	Winter
	CST 315	Fall
6	CST 347	Spring
7	CST 345	Winter

IV. Summary of 2008-09 Assessment Activities

The following are the direct assessment activities that were accomplished during 2008 - 2009 academic year. Each activity is introduced with a description of the activity followed by a table that summarized the rubric criteria along with the rubric application results. Where available, the rubric used for assessment is shown in Appendix A.

PSLO #1

The ability to apply mathematics including differential and integral calculus, probability, and discrete mathematics to hardware and software problems.

CST 162 – Introduction to Digital Logic: Fall 2008

The primary element assessed deals with the application of Boolean algebra to a mathematical construct (KMaps) for the minimization of Boolean logic expressions. This assessment focused on the application of discrete mathematics using Truth Table and Karnaugh Maps.

Data Collection Date: 11/21/2008 Coordinator: Phong Nguyen

Assessment Method: A question focusing on solving for a minimized SOP Boolean Equation was given in the CST 162 (Intro to Logic Design) test. The results of this assessment are shown in Table 4.

Performance Criteria	Measurement Scale for all criteria	Minimum Acceptable Performance Out of 15 graded	Results
	Correct/incorrect/not attempted		
K-Map:			
1.Fill out K-Map inputs ABC with correct sequences, especially the 01 to 11 transition	15/0/0	13 out of 15 – 86%	100% - Acceptable
2.Filled out K-Map correctly with required output 0's in accordance with Truth table	14/1/0	13 out of 15 – 86%	93% - Acceptable
3.Filled out K-Map correctly with required output 1's in accordance with Truth table	14/1/0	13 out of 15 – 86%	93% - Acceptable
4.Filled out K-Map correctly with required output X's in accordance with Truth table	13/2/0	13 out of 15 – 86%	86% - Acceptable
5.Change X's to correct 0's or 1's so as to best minimize expression from K-Map	12/3/0	12 out of 15 – 80%	80 % - Acceptable
6.Make correct boxes of 1' s in accordance to K-Map rules	5/10/0	12 out of 15 – 80%	33 % - NOT Acceptable
7.Translate boxes to correct product terms for minimized Boolean expression	12/3/0	12 out of 15 – 80%	80 % - Acceptable

Table 4 – Kmap assessment outcome results for CST 162: Introduction to Digital Logic

Strengths: Students are able to correctly apply the rules for construction of KMaps for deriving the KMap from a truth table and apply "don't care" conditions to gain the optimal minimization for the Boolean expression. They were also able to derive the correct Boolean expressions given a correctly formed Kmap.

Weaknesses: The major weakness is in the creation of topological groups (aka "boxing") for the forming of a minimized Boolean equation. This shows poor understanding of the mechanics of Kmaps and their correlation to Boolean algebra minimization.

Action Items: Revise CST 162 lecture material to concentrate on "boxing" of 1's and how this correlates to the minimization of Boolean algebra equations. Provide more concrete examples and discuss further the outcome of those examples.

CST 315 – Embedded Sensor and Interfacing IO: Fall 2008

The primary element assessed focused on graphical representation comprehension.

Data Collection Date: 10/24/08 Coordinator: Claude Kansaku

Assessment Method: A graph was given related to I/O interfacing on the first exam. Questions were asked requiring:

- The student to recognize the shape of the frequency response plot as that of a low-pass filter.
- The student to use a linear y-axis decibel value to determine the corresponding frequency value from the logarithmic x-axis.

The results are shown in Table 5.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Recognize the semi-log template for a passive low-pass filter	correct / incorrect	90% correct	66.7% (10/15)
Locate the cutoff frequency on the semi-log graph as defined by -3db of attenuation	correct / incorrect	70% correct	33.3% (5/15)

Table 5 – Graphical comprehension assessment for CST 315: Embedded Sensor and Interfacing IO

Strengths: Students did not perform adequately in this activity. No strength was observed.

Weakness: While the plot took a careful reading, the value could be determined accurately. A number of students specified approximate values. It is not clear why they chose that approach; either they did not know how to fully read the graph or they decided to not be accurate.

Action Items: Specify the need for accuracy.

EE221 and 223 replaces the former EET237/238. The preparation for this content will change. The question could have demanded more "precise" conclusions. The question will be re-administered and evaluated Fall 2009 as a new baseline.

CST 418 – Data Communications and Networks: Winter 2009

The primary element assessed focused on problem formulation and application of calculus.

Data Collection Date: 02/28/09 Coordinator: Douglas W. Lynn

Assessment Method: A homework question (10.6) was given in CST 418 (Networks) that required the students to solve for the optimal packet size in the transmission of a message over an N hop network. The results of this assessment are shown in Table 6.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
	Correct/Minor Errors/Incorrect		
Correct Formulation	11/0/1	70% <=1 minor error	91.7% - Acceptable
Errors in algebra	12/0/0	70% <=1 algebraic errors	100% - Acceptable
Errors in finding the derivative	12/0/0	70% <=1 error	100% - Acceptable

Table 6 – N hop assessment outcome results for CST 418: Data Communication and Networks

Evaluation 1/8/07 (date)

Strengths : Students demonstrated proficiency performance on algebra and calculus skills on this assessment. This represents an improvement over the results of this same assessment completed in the previous year where students were able to demonstrate acceptable algebra and calculus skills, but had difficulty formulating the problem in the first place (33% correctly formulated – but a small sample size of 6 students).

Weaknesses: No weakness was recorded.

Action Items: No actions need to be taken as a result of this assessment.

CST 466 – Embedded System Security: Spring 2009

This assessment was not done this year since we currently do not have a senior class in the ESET department.

PSLO #6

The ability to design, conduct and evaluate the results of experiments on embedded platforms.

CST 347 – Real-Time Operating Systems: Spring 2009

The primary element assessed was the outcome of the real-time scheduling project.

Data Collection Date: 06/05/2009 Coordinator: James Long

Assessment Method: The real-time scheduling project was collected and the outcome of the different scheduling paradigms was looked at to assess student understanding of experiment hypothesis, test creation, system implementation, and outcome explanation. The results of this assessment are given in Table 6.

Performance Criteria	Measurement Scale for all criteria	Minimum Acceptable Performance	Results
	Excellent/Good/Fair/Poor		
Hypothesis 92	0/2/0/0	100% > Good	100% - Acceptable
Test Creation 93	2/0/0/0	100% > Good	100% - Acceptable
Implementation 94	2/0/0/0	100% > Good	100% - Acceptable
Outcome 95	0/2/0/0	100% > Good	100% - Acceptable

Table 6 – Embedded experimentation assessment outcome results for CST 347: Real-time Operating Systems

Strengths: Students are strongest in creation and implementation of the tests on the embedded platform.

Weaknesses: Hypothesis creation and outcome analysis area are the weaker points; however, the two students assessed for this activity performed ok.

Action Items: We need to gather more data when more students enroll in the ESET program.

PSLO #7

The ability to analyze, design and test systems that include both hardware and software.

CST 345 – Hardware/Software Co-design: Winter 2009, 6 students.

Performance Criteria	Measurement Scale: Excellent/Good/Fair/Poor	Minimum Acceptable Performance	Results
Understands problem	5/3/0/0	100% > Good	100%
Information gathering	3/3/0/0	100% > Good	100%
HW/SW alternatives	1/4/1/0	100% > Good	83.3%
Plan to solve	2/4/0/0	100% > Good	100%
Plan implementation	1/5/0/0	100% > Good	100%
Simulation testing	1/3/2/0	100% > Good	66.7%
Prototype testing	1/4/1/0	100% > Good	83.3%

Strengths: Students met criteria performance standards for understanding the problem, information gathering, proposing hardware/software alternatives, planning solutions, implementing plans, and prototype testing.

Weaknesses: Students could not write test bench simulation code.

Action Items: Instructor will develop additional lectures on test bench code and code coverage, and will develop demonstrations on how execution of test bench code produces valid simulation test with appropriate coverage. The instructor will re-assess in winter 2010.

V. Summary of Student Learning

PSLO #1

The ability to apply mathematics including differential and integral calculus, probability, and discrete mathematics to hardware and software problems.

Strengths: Students are strong in application of algebraic and calculus for formulation and solving engineering problems.

Weaknesses: The outcome from CST 162 and CST 315 suggest that students have trouble interpreting graphical representations of problems. In both cases, students had issues with visual interpretation of graphs and the application of graphs for solving engineering problems.

Action Items: We need to emphasize the use of graphical representations of data for use in solving engineering problems. This should be done in both CST 162 and CST 315.

PSLO #6

The ability to design, conduct and evaluate the results of experiments on embedded platforms.

Strengths: Students are strongest in creation and implementation of the tests on the embedded platform.

Weaknesses: Hypothesis creation and outcome analysis area are the weaker points; however, the two students assessed for this activity performed ok.

Action Items: We need to gather more data when more students enroll in the ESET program.

PSLO #7

The ability to analyze, design and test systems that include both hardware and software.

Strengths: Students met criteria performance standards for understanding the problem, information gathering, proposing hardware/software alternatives, planning solutions, implementing plans, and prototype testing.

Weaknesses: Students could not write test bench simulation code.

Action Items: Instructor will develop additional lectures on test bench code and code coverage, and will develop demonstrations on how execution of test bench code produces valid simulation test with appropriate coverage. The instructor will re-assess in winter 2010.

VI. Changes Resulting from Assessment

The 2008 – 2009 academic year is the first for the ESET program. There are no previous results for reporting of implemented changes.

Appendix A – Assessment Rubrics

PSLO #6

The ability to design, conduct and evaluate the results of experiments on embedded platforms.
Assessed Course: CST 347 – Real-Time Operating Systems: Spring 2009

	Excellent Score = 4	Good Score = 3	Fair Score = 2	Poor Score = 1
Hypothesis 92	Hypothesis creation was clear and easy to understand.	Hypothesis had correlation to real-time systems; however, correlation was not clear.	Hypothesis was poorly formed.	Hypothesis had no correlation to desired real-time scheduling behavior.
Test Creation 93	Tests designed correlated directly to hypothesis assumptions.	Tests correlated to hypothesis; however, they were difficult to understand and results were hard to extract.	Tests partially tested hypothesis.	Test created did not test for hypothesis assumptions.
Implementation 94	Code written was easy to understand and performed designed tests.	Implementation worked and performed tests but code was pearly designed.	Implementation was buggy and performed sporadically.	Implementation was poorly done and did not perform tests.
Outcome 95	End results were analyzed and explained.	End results were analyzed; however, explanation did not draw from experimental results.	End results were enumerated with no real correlation to the hypothesis.	There was no analysis of outcome or explanation of results.

PSLO #7

The ability to analyze, design and test systems that include both hardware and software.

	1	2	3	4	Points
Understanding	Student does not have an understanding of the HW/SW Codesign problem	Student needs some clarification from others to understand the HW/SW Codesign problem	Student Understands (can explain) the HW/SW Codesign problem and proceeds to the next step	Student Understands the HW/SW problem and relates it to HW/SW Codesign solution	
Information gathering	Student does not collect any information that relates to the Codesign problem	Student collects very little information, some relates to the Codesign problem	Student collects some information, most related to the Codesign problem	Student collects a great deal of information, all relates to the Codesign problem	
Alternatives HW/SW	Student has vague or no rationale for choosing solution – has not explored other possibilities	Student has some rationale for choosing a HW/SW solution but fails to explore other possibilities	Student has an rationale for choosing a HW/SW solution but rejects of other possible HW/SW solutions	Student has an acceptable technique for developing HW/SW solution. Sound rationale explaining their choice	
Plan to Solve	Designs only one strategy, required assistance to evaluate strategy	Come up with a few strategies and requires assistance to select an appropriate strategy.	Come up with several strategies, decides on an appropriate solution	Come up with many strategies, decides on appropriate solution to each strategy.	
Carrying out the Plan	Attempts to solve Codesign problem with an inadequate HW/SW testing strategy	Solves the Codesign problem without a HW/SW testing strategy.	Solves the Codesign problem using design, makes appropriate HW/SW testing strategy	Tries new methods to solve the Codesign problem. Uses expanded HW/SW testing strategy.	
Simulation Testing & Evaluating	Student requires assistance to evaluate and test the Codesign solutions	Student has Limited evaluation of Codesign without assistance, but requires help testing Codesign solution	Student compare actual and expected results but does not repartition the HW/SW	Student suggests other modifications or applications of the results after testing the Codesign solution	
Prototype testing & Evaluation	Prototype tested with no analysis of results	Prototype tested with no analysis of results	Prototype tested including evaluation but not extensive analysis of results	Extensive analysis of testing including procedure, timing and evaluation	
Total Points					