Computer Engineering Technology
2011-12 Assessment Report

I. Introduction

In 1965, OIT was invited to join a Technical Education consortium sponsored by a number of major computer manufacturers. In response, OIT developed an Electro-Mechanical Engineering Technology program. This program was based on a mix of existing EET, MET, Math and other support courses. The name of the program was changed to Computer Systems Engineering Technology in 1973 in order to better represent the course material and capabilities of graduates. Course offerings were expanded, refined and renumbered using CST prefixes to reflect their computer systems content. Since that time, the program has continued to evolve in order to track new developments in the field and keep graduates current. As of this time, the program is only offered on the Klamath Falls campus. We currently have 84 students in the program. Retention of 2010 freshmen, sophomores and seniors within the program was 73%. We had 4 graduates this year. One graduate was awarded OITs Student Achievement award. The 2011 graduate survey shows an average graduate salary of $63,500.

II. Summary of program mission, educational objectives and student learning outcomes

The Mission, educational objectives and student learning outcomes appear below. They are reviewed and approved annually by the faculty and by our IAB members.

Mission

The mission of the Computer Engineering Technology (CET) Degree program in the Computer Systems Engineering Technology (CSET) Department at Oregon Institute of Technology is to provide an excellent education incorporating industry-relevant, applied laboratory based design and analysis to our students. The program is to serve a constituency consisting of its Alumni, employers in the high-technology industry, and the members of our IAB. Major components of the CET program's mission in the CSET Department are to:

I. educate computer engineering technology students to meet current and future industrial challenges,

II. promote a sense of scholarship, leadership, and professional service among our graduates,

III. enable our students to create, develop, and disseminate knowledge for the applied engineering environment,

IV. expose our students to cross-disciplinary educational programs, and provide high tech industry employers with graduates in the computer engineering technology profession, a profession which is increasingly being driven by advances in technology.

CET Program Educational Objectives
Program Educational Objectives are broad statements that describe the career and professional accomplishments that the program is preparing graduates to achieve.

Alumni of the Computer Engineering Technology (CET) Bachelor Degree program may be employed in a wide range of high tech industries from industrial manufacturing to consumer electronics where they will be involved in solving problems through the development of hardware, software and embedded applications. Alumni may be involved in product design, testing and qualification, application engineering, customer support, sales, or public relations.

A) Alumni will demonstrate technical competency through success in computer engineering technology positions and/or pursuit of engineering or engineering technology graduate studies if desired.

B) Alumni will demonstrate competencies in communication and teamwork skills by assuming increasing levels of responsibility and/or leadership or managerial roles.

C) Alumni will develop professionally, pursue continued learning and practice responsibly and ethically.

Alumni of the Computer Engineering Technology (CET) Associate Degree program may be employed as technicians or in support roles in a wide range of high tech industries from industrial manufacturing to consumer electronics. Alumni may be involved in product testing and qualification, customer support, sales, or public relations.

A) Alumni will demonstrate technical competence through success in computer engineering technician positions.

B) Alumni will demonstrate competencies in communication and teamwork skills through positive contributions to team based engineering projects.

C) Alumni will develop professionally, pursue continued learning and practice responsibly and ethically.

According to current statistics, one third of students who obtain the CET Associate degree also obtain a Bachelor degree in a related discipline, most often a Bachelor degree in Software. In this case, the Associate degree adds breadth to their education. Alumni in this category would be expected to perform at a level consistent with the Bachelor degree program educational objectives.

CET Bachelor of Science Program Student Learning Outcomes

Graduates of the CET Bachelor's degree program are expected to be able to demonstrate:

(1) an ability to identify, formulate, and solve computer engineering technology problems, including the specification, design, implementation, and operation of systems and components, that meet performance, and quality requirements in a timely manner (Objective A & C) ;

(2) an ability to design, conduct, and interpret experiments including applying the results to verify the system (Objective A);

(3) an ability to function effectively on teams (Objective B);

(4) an understanding of professional, ethical and social responsibility (Objective C);

(5) a recognition of the need for, and an ability to engage in, life-long learning (Objective C).

(6) the ability to apply mathematics including differential and integral calculus, probability, and discrete mathematics to hardware and software problems (Objective A);

(7) mastery of the techniques, skills, and knowledge appropriate to the degree program, with depth in at least two sub disciplines (microprocessors, ASICs, software, computer architecture) of the computer engineering technology program (Objective A);

(8) an ability to use applied engineering tools, techniques, and skills including computer-based tools for design, analysis and simulation (Objective A);

(9) an ability to design, fabricate and test systems containing hardware and software components; as well as to analyze and interpret test results in order to improve the system (Objective A);

(10) an ability to convey technical material through oral presentation and interaction with an audience (Objective B);

(11) an ability to convey technical material through written reports which satisfy accepted standards for writing style (Objective B);

(12) an ability to improve system design with regard to quality and project management (Objective A).

CET Associate Degree Student Learning Outcomes

Graduates of the CET Associate degree program are expected to be able to demonstrate:

(1) an ability to identify, formulate, and solve computer engineering technology problems, including the test, implementation, and operation of systems and components, that meet performance and quality requirements in a timely manner (Objective A & C) ;

(2) an ability to design, conduct, and interpret experiments including applying the results to verify a system (Objective A);

(3) an ability to function effectively on teams (Objective B);

(4) an understanding of professional, ethical and social responsibility (Objective C);

(5) a recognition of the need for, and an ability to engage in, life-long learning (Objective C).

(6) the ability to apply mathematics including differential and integral calculus and discrete mathematics to hardware and software problems (Objective A);

(7) an ability to use applied engineering tools, techniques, and skills including computer-based tools for analysis, simulation, and testing (Objective A);

(8) an ability to fabricate and test engineering systems containing hardware and software components (Objective A);

(9) an ability to convey technical material through oral presentation and interaction with an audience (Objective B);

(10) an ability to convey technical material through written reports which satisfy accepted standards for writing style (Objective B);

III. Assessment Cycle

The current assessment cycle appears below. For the BS program, four of the 12 student learning outcomes are assessed each year of a three year cycle. For the AE program, the outcomes that correspond to the BS program outcomes are assessed.

CET BS Program Assessment Plan – 2011-12

Learning Outcome	2011-12	2012-13	2013-14
(1) an ability to identify, formulate, and solve computer engineering technology problems, including the specification, design, implementation, and operation of systems and components, that meet performance, and quality requirements in a timely manner;			•
(2) an ability to design, conduct, and interpret experiments including applying the results to verify the system;	•		
(3) an ability to function effectively on teams;		•	
(4) an understanding of professional, ethical and social responsibility;		•	
(5) a recognition of the need for, and an ability to engage in, life-long learning.			•
(6) the ability to apply mathematics including differential and integral calculus, probability, and discrete mathematics to hardware and software problems;	•		
(7) mastery of the techniques skills, and knowledge appropriate to the degree program, with depth in at least two sub disciplines (microprocessors, ASICs, software, computer architecture) of the computer engineering technology program;		•	
(8) an ability to use applied engineering tools, techniques, and skills including computer-based tools for design, analysis and simulation;	•		
(9) an ability to design, fabricate and test systems containing hardware and software components; as well as to analyze and interpret test results in order to improve the system;	•		
(10) an ability to convey technical material through oral presentation and interaction with an audience;			•
(11) an ability to convey technical material through written reports which satisfy accepted standards for writing style;			•
(12) an ability to improve system design with regard to quality and project management		•	

CET AS Program Assessment Plan – 2011-12

Learning Outcome	2011-12	2012-13	2013-14
(1) an ability to identify, formulate, and solve computer engineering technology problems, including the test, implementation, and operation of systems and components, that meet performance and quality requirements in a timely manner;			•
(2) an ability to design, conduct, and interpret experiments including applying the results to verify a system;	•		
(3) an ability to function effectively on teams;		•	
(4) an understanding of professional, ethical and social responsibility;		•	
(5) a recognition of the need for, and an ability to engage in, life-long learning;			•
(6) the ability to apply mathematics including differential and integral calculus and discrete mathematics to hardware and software problems;	•		
(7) an ability to use applied engineering tools, techniques, and skills including computer-based tools for analysis, simulation, and testing;	•		
(8) an ability to fabricate and test engineering systems containing hardware and software components;	•		
(9) an ability to convey technical material through oral presentation and interaction with an audience;			•
(10) an ability to convey technical material through written reports which satisfy accepted standards for writing style			•

IV. Summary of 2011-12 Assessment Results

During the 2011-12 academic year, the program faculty assessed four student learning outcomes as summarized below. These outcomes are mapped to the CET curriculum in Appendix A. Additional information can be found in department assessment records.

Student Learning Outcome #2 (B.S. and A.E. degrees): An ability to design, conduct, and interpret experiments including applying the results to verify the system.

Indirect Assessment #1
Data Collection Date: 6/6/12
3 of 3 students responding to the senior exit survey indicated they strongly agreed that they were highly prepared in this learning outcome. The question options were: Strongly disagree, Disagree, Agree, and Strongly agree.

Direct Assessment #1
Data Collection Date: 3/15/12
Coordinator: Douglas W. Lynn

Assessment Method: Students in the CST 331 lab were asked to determine if the PIC32s PMP address auto increment feature was a pre or post-increment. To answer this question, students needed to setup a simple experiment and interpret the results. There are a number of ways the experiment can be setup. Students usually setup the PMP for an access with auto increment and then observed the behavior of the PMP address bus on a logic analyzer.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Correct experiment design	yes / no	70% correct	100% correct (5/5 correct)
Correct result	yes / no	70 % correct	100% correct (5 / 5 correct)

Evaluation 5/30/12: Students demonstrated that they are able to conceive and carry out an experiment to answer a question.
Actions 5/30/12: No changes need to be made as a result of this evaluation.

Direct Assessment #2
Data Collection Date: 3/19/12
Coordinator: Ralph Carestia

Assessment Method: Students in CST 345 (Hardware/Software Codesign) were given a laboratory problem where they had to develop an IP for a keypad and construct an interrupt

driven keypad controller for PicoBlaze microcontroller, simulate the design and test it in the Xilinx ISE/Modelsim environment. They were to synthesize the design with Xilinx or Mentor Graphics Precision CAE tool, analyze and simulate the results with Modelsim. Finally they had to create the integrated logic analyzer (ILA and ICON core) and use ChipScope-Pro to analyze the results. The experiment in this case was to setup the virtual logic analyzer in order to measure the interrupt latency. Even though other learning outcomes could have been used, this problem was primarily evaluated, assessed and analyzed under student learning outcome #2, focusing on testing the interrupt response timing of the system.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Knowledge	Percent at excellent or good levels	70% excellent or good	75% (6 / 8)
Analysis	"	"	50% (4 / 8)
Fabrication	"	"	100% (8 / 8)
Testing	"	"	50% (4 / 8)
Test Interpretation	"	"	50% (4 / 8)

Evaluation 5/30/12: Students did well in their ability to understand the problem and gather information. However the juniors in the class struggled in developing a plan to solve, develop the Verilog code for the solution. All were able to fabricate the design, however this was a minimal problem in this case since most of the design is inside the chip. The juniors struggled in the area of being able test the design; however the seniors were able to test appropriately due to having more experience in testing from the additional classes that they had. Juniors need to have additional instruction in carrying out a procedure for testing and being able to interpret, evaluate results, and make changes from those results. Seniors have had CST 351 and 331 prior to taking the class. The juniors in this class are embedded students and they have only been exposed to logic analyzers in CST 337 where the triggering is simple.

Actions 5/30/12: It appears that at the junior level students need additional work in testing. Senior students in the class were able to handle this without a problem – the senior duals had software testing and hardware testing in classes prior to the CST345 class. We will add depth in triggering for the logic analyzer in CST 337 for embedded students. Part of this will improve automatically when we get new logic analyzers (more tuned to serial interfaces) for CST 337. This would give more opportunity for complex triggering.

Student Learning Outcome #6 (B.S. and A.E. degrees): The ability to apply mathematics including differential and integral calculus, probability, and discrete mathematics to hardware and software problems.

Indirect Assessment #1
Data Collection Date: 6/6/12
3 of 3 students responding to the senior exit survey indicated they agreed that they were highly prepared in this learning outcome. The question options were: Strongly disagree, Disagree, Agree, and Strongly agree.

Direct Assessment #1
This assessment focused on the application of discrete mathematics using Truth Tables and Karnaugh Maps.
Data Collection Date: 11/11/11
Coordinator: Phong Nguyen

Assessment Method: A question focusing on solving for a minimized SOP Boolean Equation from a 4-variable truth-table was given in the CST 162 (Intro to Logic Design) as a quiz. The following table provides the results

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
1. Construct the K-Map properly, especially the 01 to 11 transition	correct / incorrect or not attempted)	85% correct	97.6% (41/42)
2. Enter 1's, 0's and don't cares correctly into the K-map	correct / incorrect (or not attempted)	85% correct	90.5% (39/42)
3. Make correct loops of 1' s in accordance with K-Map rules	correct / incorrect (or not attempted)	80% correct	35.7% (15/42)
4. Properly include don't cares in loops so as to arrive at a minimal expression	correct / incorrect (or not attempted)	80% correct	81% (34/42)
5. Properly translate loops to product terms.	correct / incorrect (or not attempted)	80% correct	81% (34/42)

Evaluation 4/18/12: The performance was acceptable in 4/5 criteria. The majority of incorrect loops was due to one redundant loop being included in the final expression (due to the difficulty of the problem). These results were similar to the previous cycle's assessment of this outcome.

Actions 4/18/12: Overall the performance was judged acceptable. In the previous assessment cycle, we recommended increasing the lecture time devoted to this topic. This recommendation was implemented, but it did not improve performance on criteria 3. Giving a quiz or additional homework exercise prior to the assessment may point out the importance of considering redundant loops.

Direct Assessment #2
This assessment focused on computation.
Data Collection Date: 12/07/11
Coordinator: Douglas W. Lynn

Assessment Method: An exam question was given on the CST 344 final that asked the students to convert a decimal number to IEEE 754 floating point format. Part of this problem required students to convert a decimal fraction to a binary fraction – something their calculators do not directly do.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Correct Method and Result	number of errors	70% <=1 minor error	100% <=1 minor error 6/6 correct

Evaluation 4/18 /12: Students demonstrated proficiency on this task.
Actions 4/18 /12: No changes need to be made as a result of this evaluation.

Direct Assessment #3
This assessment focused on problem formulation.
Data Collection Date: 02/08/12
Coordinator: Douglas W. Lynn

Assessment Method: A question (6d) was given on the CST 442 midterm exam that required students to compute the change in CPI from making jumps take one cycle as opposed to two. To correctly solve this problem, students have to realize that CPIold = $1.17 = x + .02 \times 2$, and that what they want is CPInew = $x + .02 \times 1 = 1.17 - .02 \times 1 = 1.15$.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Correct Formulation	number of errors	60% correct formulation	83.3% had a correct formulation 5 / 6

Evaluation 4/18/12: Performance exceeded expectations, doing much better than the last time this assessment was given.
Actions 4/18/12: No changes need to be made as a result of this assessment.

Direct Assessment #4
This assessment focused on problem formulation and application of calculus.
Data Collection Date: 03/16/12
Coordinator: Douglas W. Lynn

Assessment Method: A homework question (10.6) was given in CST 418 (Networks) that required the students to solve for the optimal packet size in the transmission of a message over an N hop network. Students were informed that the results would be used for assessment, and that they were to do their own work and not use any symbolic algebra tools.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Correct Formulation	number of errors	70% <=1 minor error	100% <=1 minor error 5/5 correct
Errors in algebra	number of errors	70% <=1 algebraic errors	100% 5/5 correct algebraically
Errors in finding the derivative	number of errors	70% <=1 error	100% 5/5 correct

Evaluation 4/18/12: Students exceeded expectations on algebra and calculus skills on this assessment.

Actions 4/18/12: No actions need to be taken as a result of this assessment.

Direct Assessment #5
This assessment focused on the application of basic probability.
Data Collection Date: 3/20/12
Coordinator: Douglas W. Lynn

Assessment Method: The following question was given in the CST 418 (Networks) final exam: If the probability of an error in one packet of a message traversing one hop of a network is Pe, what is the probability that N packets can be delivered across an n hop virtual circuit without any errors? To correctly solve this problem students must realize that Pne = 1 - Pe, that N x n packets have to be transmitted without error and that probabilities multiply.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Pne = 1 - Pe	correct / incorrect (or not attempted)	85% correct	100% (5/5)
Probabilities multiply	correct / incorrect (or not attempted)	85% correct	100% (5/5)

Evaluation 4/18/12: Performance exceeded expectations.

Actions 4/18/12: No changes need to be made as a result of this assessment.

Direct Assessment #6
This assessment focused on graphical comprehension.
Data Collection Date: 9/14/12
Coordinator: Claude Kansaku

Assessment Method: A question was given in the first exam of CST 335. The question presented a semi-log graph of the frequency response of a low-pass filter without identifying it as such. The student must be able to recognize the shape of the frequency response plot as that of a low-pass filter. Furthermore, the student must be able to use a linear y-axis decibel value to determine the corresponding frequency value from the logarithmic x-axis.

Background: This content is primarily covered in prerequisite electronics classes. However, it is reviewed in CST 335 as an introduction to signal characteristics. The first lab was to manually measure the response of a passive low-pass filter. Students input a series of sinusoidal signals of a fixed amplitude. They were required to measure the output amplitude at each frequency and plot the values converted to decibels on a semi-log graph. This exam question tested their comprehension of that material.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Recognize the semi-log template for a passive low-pass filter	correct / incorrect	80% correct	83.33% (10/12)
Locate the cutoff frequency on the semi-log graph as defined by -3db of attenuation	correct / incorrect	70% correct	16.67% (2/12)

Evaluation 9/19/12: The performance did not meet expectations. Students are able to identify the form of the graph but not able to read numerical details on the graph itself.

Actions 9/19/12: For reasons outside of this assessment, the CET program has implemented a different AC circuits course. As a result, future students will have more opportunity to read and process filter response presented on semilog graphs. It is hoped that this change will help students make precise readings from semilog graphs.

Direct Assessment #7
Data Collection Date: 9/14/12
Coordinator: Claude Kansaku

Assessment Method: A question was given in the first exam of CST 335. The question presented a problem that required students to setup and integral to compute the average value of a function.

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Formulate the integral	correct / incorrect	70% correct	83.33% (10/12)
Correctly derive the average	correct / incorrect	70% correct	58.33% (7/12)

Evaluation 9/19/12: Based on how the question was worded, it appears that students are able to follow written directions and setup an integral. However, it appears that most do not know how to apply the appropriate rules of calculus to compute a numerical result.

Actions 9/19/12: The instructor who collected the data will consult with a mathematics faculty member to see if he/she would have expected the students to have arrived at correct results. Then we will explore possible corrections in conjunction with mathematics faculty.

Student Learning Outcome #8 (B.S. Degree) An ability to use engineering tools, techniques, and skills including computer-based tools for design, analysis and simulation.
Student Learning Outcome #7 (A.E. Degree) An ability to use engineering tools, techniques, and skills including computer-based tools for analysis, simulation, and testing.

Indirect Assessment #1
Data Collection Date: 6/6/12
3 of 3 students responding to the senior exit survey indicated they agreed or strongly agreed that they were highly prepared in this learning outcome. The question options were: Strongly disagree, Disagree, Agree, and Strongly agree.

Direct Assessment #1
Data Collection Date: Fall term 2011
Coordinator: Claude Kansaku, Phong Nguyen

Students were observed in CST 162 labs using graphical design entry for PLD designs.

Evaluation 5/30/12: Performance exceeded expectations. The professors noted no students having problems accomplishing this task.

Actions 5/30/12: No changes need to be made as a result of this assessment.

Student Learning Outcome #9 (B.S. degree) An ability to design, fabricate and test systems containing hardware and software components; as well as to analyze and interpret test results in order to improve the system.
Student Learning Outcome #8 (A.E. degree) An ability to fabricate and test engineering systems containing hardware and software components;

Indirect Assessment #1
Data Collection Date: 6/6/12
2 of 3 students responding to the senior exit survey indicated they agreed or strongly agreed that they were highly prepared in this learning outcome. 1 disagreed. The question options were: Strongly disagree, Disagree, Agree, and Strongly agree.

Direct Assessment #1
Data Collection Date: 3/20/12
Coordinator: Ralph Carestia

Assessment Method: Sophomore students in the CST 232 (Programmable Logic) were given a laboratory problem where they were required to be read input from a keypad and display the corresponding button pressed onto a seven segment display. The BCD character was to be displayed in the least significant position and shifted over when a new key was entered. Quartus was used to compile and simulate the design. The results were then tested using functional simulation and viewed on test equipment. (Didn't test well enough to handle key lockout.)

Performance Criteria	Measurement Scale	Minimum Acceptable Performance	Results
Knowledge (Understanding how to design the hardware)	Percent at excellent or good levels	70% excellent or good	85.7% (12 / 14)
Implementation (Carries out the Design)	"	"	85.7% (12 / 14)
Fabrication (Skill in fabrication)	"	"	78.6% (11 / 14)
Testing (Uses appropriate methods for testing)	"	"	64.3% (9 / 14)

Evaluation 5/30/12: Performance exceeded expectations in all but the Testing area. Students did well in their ability to understand the problem and in gathering the information needed to implement the design in most cases. Most students were able to develop the Verilog code for the solution. However they struggled in developing a plan for testing and following through on the plan and neglected to test using the simulator before implementing on their boards. They were able to fabricate the design on their boards, but their schematics lacked information. They also struggled in the physical testing and required help in interpreting the results.

Actions 5/30/12: It appears that at the sophomore level, students need additional work in testing. Testing is first introduced in CST 231/2. Students may get more exposure to test equipment when we add the class in instrumentation next year, since they seem to struggle in using the test equipment. They also learn more about testing in the junior year. Next time this assessment comes up, we will also assess in CST 351.

Direct Assessment #2
Data Collection Date: 6/9/12
Coordinator: Phong Nguyen

Assessment Method: This assessment is based on the design life cycle of 4 different devices developed by the 4 teams in the three term Junior Project.

Performance Criteria	Measurement Tool	Minimum Acceptable Performance	Results
Proposal (input, processing, control, memory, output, wireless communications)	Proposal paper and rubric	100% of teams must satisfy all criteria in the rubric	100% (4 / 4)
Plan for design, schedule, control	Plan/schedule/ control folder and rubric	70% of teams must satisfy 80% or more of the rubric criteria	75% (3 / 4)
Fabrication	Project device fabricated from proposal/plan	100% of teams must fabricate devices according to plan	100% (4 / 4)
Functional testing	Actual devices and final hardware/ software check-off rubric	70% of team's devices functionally tested and achieving 80% of proposal specifications by 2nd quarter	75% (3 / 4)
Improvement	Paper describing improvement of one aspect of the final design. Rubric given	100% of papers achieving 80% of the requirements of the rubric	100% (4 / 4)

Evaluation 6/9/12: All projects met acceptable criteria

Actions 6/9/12: No changes need to be made as a result of this assessment

V. Summary of Student Learning

Student Learning Outcome #2 (BS and AE) an ability to design, conduct, and interpret experiments including applying the results to verify the system;

It appears that hardware and dual students were able to setup and interpret experiments. Embedded Juniors (who received less exposure to testing because they do not take CST 331) had problems constructing triggers for the logic analyzers.

Student Learning Outcome #6 (BS and AE) the ability to apply mathematics including differential and integral calculus, probability, and discrete mathematics to hardware and software problems;

Assessment results in this area improved over the last time these assessments were done. However it appears that freshman still have trouble with redundant product terms, juniors have problems reading data from semi-log graphs and problems solving an integral. Seniors, however, appear to be able to manage probability, semi-log graphs and calculus adequately.

Student Learning Outcome #8 (BS) an ability to use engineering tools, techniques, and skills including computer-based tools for design, analysis and simulation;
Student Learning Outcome #7 (AE) an ability to use engineering tools, techniques, and skills including computer-based tools for analysis, simulation, and testing;

The one assessment conducted for this outcome showed no problems. As a result of the assessment done for outcome 2, it appears that junior embedded students may not have enough exposure to triggering on logic analyzers. Based on general faculty observation, students are adequately prepared to use logic analyzers, oscilloscopes as well as simulators and design capture programs and tools by the time they graduate.

Student Learning Outcome #9 (BS) an ability to design, fabricate and test systems containing hardware and software components; as well as to analyze and interpret test results in order to improve the system;
Student Learning Outcome #8 (AS) an ability to fabricate and test engineering systems containing hardware and software components;

Juniors demonstrated proficiency on this outcome, but sophomores struggled with testing and interpreting test results. One senior (out of 3) indicated that he didn't feel prepared in this learning outcome on an indirect assessment.

VI. Changes Resulting from Assessment

Seniors did better on algebra, calculus, and probability problems in this assessment cycle As a result of assessment we decided we need yet more preparation in CST 130 (an additional quiz or assignment) on recognizing redundant terms and additional work with logic analyzer triggering in CST 337. As a result of other assessment, we had already decided to implement an instrumentation lab. The need for this was also underscored by this year's assessment results. Also, the implementation of a different AC circuits class will give us the opportunity to bolster student's skills with interpreting semi-log frequency responses. In conjunction with mathematics

faculty, we will pursue possible reasons behind juniors apparent inability to solve integral problems, and implement an appropriate response.

Appendix A: SLO Curriculum Maps

Outcome Assessment Points, BS Program H = Highly assessable M = Weakly assessable blank = Low to not assessable		(1) problem solving	(2) experiment	(3) teamwork	(4) ethical / social resp	(5) life-long learning	(6) calc, prob, discrete	(7) master skills + knowledge	(8) design, analysis, sim	(9) design, fab, test, improve	(10) oral presentation	(11) written presentation	(12) quality, proj. manage
Freshman Year	Eval. Cycle ⇨	Y1	Y2	Y1	Y3	Y2	Y1	Y3	Y2	Y1	Y3	Y2	Y3
CST 102	Intro to Comp ET	M	M	M	M					M		M	
CST 162	Intro to Digital Logic	H	M				M						
MATH 111	College Algebra												
WRI 121	English Comp												
CST 116	C++ Prog I												
CST 130	Computer Org						M						
MATH 112	Trigonometry												
WRI 122	English Comp												
CST 126	C++ Prog II												
CST 131	Comp Arch						M						
MATH 251	Diff Calculus						M						
SPE 111	Fund of Speech										M		
SSC	SS Elective												
Sophomore Year													
CST 250	Assembly Lang												
MATH 252	Integral Calculus						M						
PSY 201	Psychology												
WRI 227	Tech Report											M	
CST 133	Dig Elec II – Seq w HDL						M			M			
CST 204	Intro to µcontrollers						M		M	M			
EE 221	DC & 1st Ord Trans												
CST 231/2	Comp Des w/PLD	M	H			M	M		M	H			
MATH 254N	Vector Calc						H						
CST 313	Comp Soft Tech	M	M				M	M	M	M			
EE 223	AC & 2nd Ord Trans												
SPE 321	Team Comm			M							H		
HUM	Hum Elective												
MATH	Math Elective						H						

Outcome Assessment Points, BS Program continued		(1) problem solving	(2) experiment	(3) teamwork	(4) ethical / social resp	(5) life-long learning	(6) calc, prob, discrete	(7) master skills + knowledge	(8) design, analysis, sim	(9) design, fab, test, improve	(10) oral presentation	(11) written presentation	(12) quality, proj manage
Junior Year	Eval. Cycle ⇨	Y1	Y2	Y1	Y3	Y2	Y1	Y3	Y2	Y1	Y3	Y2	Y3
EE 321	Intro Amp & Semi												
CST 335	I/O Interfacing	M	M	M		M				M			
CST 371	Embedded Sys Dev I	H	M	H		M			H	M	H	H	M
PHY 221	Physics w/Calculus												
CST 321	Intro to □proc	M	M				M	M	M	M		H	
CST 372	Embedded Sys Dev II	H	M	H		M	M	M	H	H	M	M	M
PHY 222	Physics w/Calculus												
WRI 327	Adv Tech Writing											H	
CST 331	Microproc Interface	M	M				M	M	M	M		M	
CST 351	Advanced PLDs	H	H		M	M		M	H	M			M
CST 373	Embedded Sys Dev III	H	H	H	M	H	M	M	M	H	H	H	H
PHY 223	Physics w/Calculus												
HUM	Hum Elective				M								
Senior Year													
BUS 304	Engr Management				M								
CST 344	Intermediate Arch	M			M		M	M	M	M			
CST 441	Logic Synth w VHDL	H	H		M	M		H	H	M			
CST 418	Data Comm & Net	M				M	H						
CST xxx	Tech Elective					M							
CST 442	Advanced Arch.	M				M	H	H	M	M			
CST 451	ASIC Des using FPGAs	H	H		M	M		H	M	H	H	H	M
SSC	SS Elective				M								
IMGT 345	Engr Economy				M								M
CST 464	RISC-Based µproc	M	M	M		M		M	M	M			
CST 461	Adv Topics in VLSI	M	H				M	H	H			M	
PSY 347	Org Behavior				M								
HUM	Hum Elective				M								

Outcome Assessment Points, AE Progam H = Highly assessable M = Weakly assessable blank = Low to not assessable		(1) problem solving	(2) experiment	(3) teamwork	(4) ethical / social resp	(5) life-long learning	(6) calc, discrete	(7), analysis, sim, test	(8) fabricate, test	(9) oral presentation	(10) written presentation
Freshman Year	Eval. Cycle ⇨	Y1	Y2	Y1	Y3	Y2	Y1	Y2	Y1	Y3	Y2
CST 102	Intro to Computer Eng. Tech.	M	M	M					M		M
CST 162	Intro to Digital Logic	H	M				M				
MATH 111	College Algebra										
WRI 121	English Composition										
CST 116	C++ Programming I										
CST 130	Computer Organization						M				
MATH 112	Trigonometry										
WRI 122	English Composition										
CST 126	C++ Programming II										
CST 131	Computer Architecture						M				
MATH 251	Differential Calculus						M				
SPE 111	Fundamentals of Speech									M	M
SSC	Social Science Elective										
Sophomore Year											
CST 250	Computer Assembly Language										
MATH 252	Integral Calculus						M				
PSY 201	Psychology										
WRI 227	Technical Report Writing										M
CST 133	Dig. Elec. II – Seq. Logic w HDL						M				
CST 204	Introduction to µcontrollers						M				
EE 221	Circ. I – DC & 1st Order Trans.										
CST 231	Computer Design w/PLD	M	H			M	M	M	H		
CST 232	Comp. Design w/PLD Lab	H	H			M	M	M	H		
PHY 221	General Physics w/Calculus										
CST 313	Comp Software Techniques	H	M	H			M	M	M		M
EE 223	Circ. II – AC & 2nd Order Trans.										
PHY 222	General Physics w/Calculus										
HUM	Humanities Elective				M						
CST xxx	Technical Elective**					M					